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REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1-13 are pending in the application. Claims 1-13 have been rejected. Claim 1 has been cancelled without prejudice or disclaimer. Claim 2 has been amended. Applicants respectfully assert that the amendments to the claims add no new matter.

Interview Summary

Applicants thank the Examiner for the courtesy of the Telephonic Interview with applicants' representatives on April 14, 2005.

In the interview, dated April 14, 2005, the 35 U.S.C. § 101 rejection of claim 2 was discussed and it was agreed to amend claim 2 by adding the limitation of "in a digital signal processor" as detailed below.

35 U.S.C. § 101 Rejections

In the Office Action, the Examiner rejected claims 1-8 under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Claim 1 has been deleted and therefore the rejection to this claim is now moot.

Claim 2 has been amended to include "performing a first cycle in a digital signal processor" and "performing a second cycle in a digital signal processor".

Accordingly, the claim includes a limitation to a practical application, and/or requires a specific computer to implement the claimed process.

Accordingly, Applicants respectfully request that the rejection of claims 2-8 under 35 USC 101 be withdrawn.

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35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claims 1-13 under 35 U.S.C. § 103(a), as being obvious over Lim et al. (U.S. 6,463,451) in view of Shridhar et al (U.S. 6,366,937).

Applicants respectfully traverse the rejection.

An obviousness rejection requires a teaching or a suggestion by the relied upon prior art of all the elements of a claim (M.P.E.P. §2142).

Claim 9 recites: “*in a first cycle said first multiplier is to multiply a real sinusoidal data input of a Fast Fourier Transform butterfly calculation and an imaginary coefficient of said butterfly calculation and said second multiplier is to multiply an imaginary sinusoidal data input of said butterfly calculation and a real coefficient of said butterfly calculation, and where in a second cycle said first multiplier is to multiply a real sinusoidal data input of a next butterfly calculation and a real coefficient of said next butterfly calculation and said second multiplier is to multiply an imaginary sinusoidal data input of said next butterfly calculation and an imaginary coefficient of said next butterfly calculation*”

Claim 2 recites: “*in a first cycle: adding... to a first product...and subtracting therefrom a second product”...; and adding ...to said second product and subtracting therefrom said first product; and in a second cycle: adding... to a third product...and to a fourth product”...; and subtracting from ... said third product and said fourth product”.*

Claim 9 further recites “*a first three-input arithmetic logic unit*” and “*a second three-input arithmetic logic unit*”.

Applicant asserts that neither Lim et al nor Shridhar, alone or in combination, teaches or suggests claims 2 and 9, as discussed below.

Lim et al. discloses a conventional method of performing a Fast Fourier Transform (FFT) butterfly calculation and the Examiner stated that Lim does not disclose performing FFT in 2 cycles.

Shridhar et al. discloses a method that implement a butterfly operation for a FFT operation in a processor using a matrix-vector-multiply instruction (see abstract). Shridhar et al. discloses using matrix arithmetic for the calculation of a butterfly, multiplying a 4x4

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matrix with a 4x1 vector. The result of this multiplication is then stored back into the same vector, for the calculation of the following FFT butterfly operation. Therefore, Sridhar et al. discloses, using sixteen multiplications for a single butterfly operation, which is a completely different method than the method claimed in claim 2 reciting a first and second product for the first cycle and a third and a fourth product for the second cycle (four multiplications).

Sridhar et al. further discloses using 4-input adders (see Fig. 3 of Shridhar) for the butterfly calculation, namely, 3 operations of adding or subtracting 4 elements are used in order to accomplish a complete FFT calculation. Shridhar uses this technique, which is suitable for floating-point calculations and floating-point vector processors. In contrast, claim 9 recites “a first three-input arithmetic logic unit” and “a second three-input arithmetic logic unit”.

Additionally, in the office Action, the Examiner contends that that “*it would have been obvious to apply and arrange the 4-point FFT to perform within 2 cycles only, wherein the first cycle processes four multiplications, two additions, and two subtractions for the first and second result; and a second cycle processes another four multiplications, two additions, and two subtractions for the third and fourth results using the pipelined instruction device in Shridhar et al.’s invention into Lim et al.’s invention*”. Applicant respectfully asserts that the teaching described above is different than what is claimed in 2 and 9 of the subject application.

As discussed above, claims 2 and 9 claim a method and a processor that use 2 multiplications in a first cycles and 2 multiplications in a second cycle and the combination of Lim et al. and Shridhar et al. does not teach or suggest the claims 2 and 9.

Therefore, Applicant asserts that Lim et al. and Shridhar et al., alone or in combination, fail to teach or suggest all limitations of claims 2 and 9.

Claims 2–8 and 10 – 13 are each dependent, directly or indirectly, from either claim 2 or claim 9 and includes all the limitations of this claim. Therefore, it is respectfully submitted that claims 2–8 and 10 – 13 are patentable at least for the reasons set forth above.

Therefore, it is respectfully requested that the rejection of claims 2 - 13 under 35 USC §103(a) be withdrawn.

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Double Patenting Rejections

In the Office Action, the Examiner rejected claim 1 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims U.S. 6,625,630.

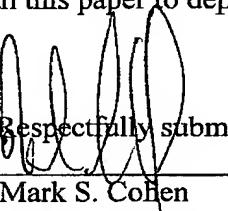
Claim 1 has been cancelled and therefore the double patenting rejection is now moot.

Conclusions

In view of the foregoing amendments and remarks, the pending claims are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 50-3355.

Respectfully submitted,


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